

METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

ABSTRACT OF THE DISCLOSURE

- 5 The present invention provides different schemes for reducing the size (such as thickness) of at least a semiconductor unit (such as an IC chip) which is to be packaged. It replaces, in packaging at least a semiconductor unit, conventional grinding processes by etching schemes, particularly when the thickness of the semiconductor unit approximates
- 10 an expected specification. The etching process may be embodied in a way that a semiconductor unit attached to a carrier such as a substrate, or placed onto a seating apparatus such as a chip tray, and properly shielded, is etched by means of using gas such as plasma, or beams of light. The semiconductor unit packaged according to the scheme provided by the
- 15 present invention can thus be immunized against the failure resulting from die crack or back-side chipping.

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